1kHz-3GHz High Signal Level Active Mixer

FEATURES

- **Broadband RF, LO and IF Operation**
- **High Input IP3: >20dBm from 30MHz to 900MHz**
  +17dBm at 1900MHz
- **Typical Conversion Gain: 1dB**
- **SSB Noise Figure: 11dB at 900MHz**
  14dB at 1900MHz
- **Integrated LO Buffer: Insensitive to LO Drive Level**
- **Single-Ended or Differential LO Drive**
- **High LO-RF Isolation**
- Enable Function
- 4.5V to 5.25V Supply Voltage Range
- 4mm × 4mm QFN Package

APPLICATIONS

- HF/VHF/UHF Mixer
- Cellular/PCS/UMTS Infrastructure
- High Linearity Mixer Applications
- ISM Band Receivers
- Wireless Medical Telemetry System (WMTS)

DESCRIPTION

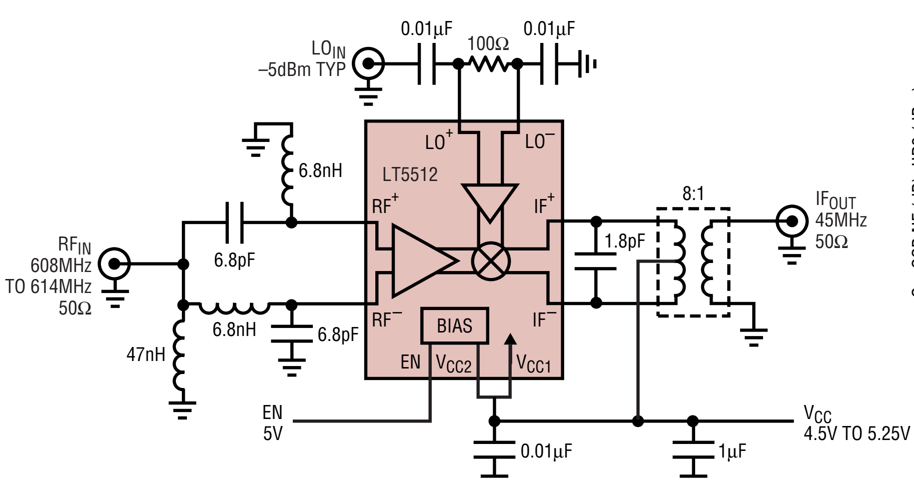
The LT®5512 is an active double-balanced mixer IC, optimized for high linearity HF, VHF and UHF applications. The IC includes an integrated LO buffer amplifier to drive the mixer and an RF buffer amplifier for improved LO-RF isolation. Internal bias circuits eliminate the need for precision external resistors and allow the device to be powered-down using the enable control (EN) pin.

The externally matched RF and IF ports allow the mixer to be used at very low frequencies, below 1MHz or up to 3GHz. The differential LO input is designed for single-ended or a differential input drive.

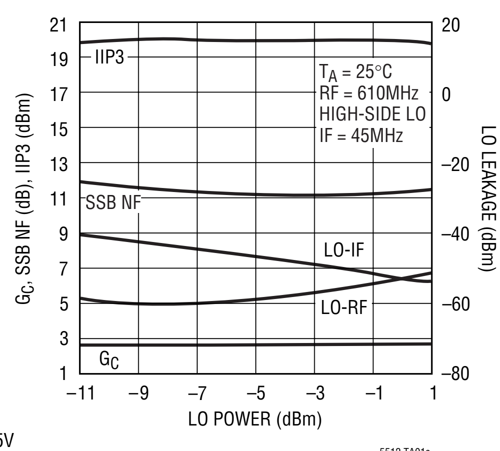
The LT5512 is a high-linearity alternative to passive diode mixers. Unlike passive mixers, which have conversion loss and require high LO drive levels, the LT5512 delivers conversion gain and requires significantly lower LO drive levels.

TYPICAL APPLICATION

High Signal-Level Downmixer for 600MHz Wireless Medical Telemetry System



Conv Gain, IIP3, NF and LO Leakage vs LO Power



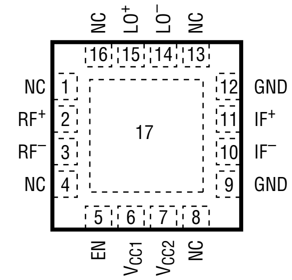
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC1}, V_{CC2}, IF^+, IF^-)........................5.5V
Enable Voltage ....–0.3V to V_{CC} + 0.3V
LO^+ to LO^- Differential Voltage ....±1.5V
....(+6dBm equivalent)
RF^+ to RF^- Differential Voltage...............................±0.7V
....(+11dBm equivalent)
Operating Temperature Range ....–40°C to 85°C
Storage Temperature Range...................–65°C to 125°C
Junction Temperature (T_J) .... 125°C

PACKAGE/ORDER INFORMATION

TOP VIEW



UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD IS GROUND (PIN 17)
(MUST BE SOLDERED TO PCB)

ORDER PART NUMBER	PART MARKING
LT5512EUF	5512

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

DC ELECTRICAL CHARACTERISTICS

(Test Circuit Shown in Figure 2) V_{CC} = 5V, EN = High, T_A = 25°C (Note 3), unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Enable (EN) Low = Off, High = On					
Turn On Time			3		µs
Turn Off Time			13		µs
Input Current	V_{ENABLE} = 5V		50		µA
Enable = High (On)		3			V
Enable = Low (Off)				0.3	V
Power Supply Requirements (V_{CC})					
Supply Voltage		4.5		5.25	V
Supply Current			56	74	mA
Shutdown Current	EN = Low			100	µA

AC ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RF Input Frequency Range	Requires Appropriate Matching		0.001 to 3000		MHz
LO Input Frequency Range	Requires Appropriate Matching		0.001 to 3000		MHz
IF Output Frequency Range	Requires Appropriate Matching		0.001 to 2000		MHz
LO Input Power	1kHz to 1700MHz (Resistive Match) 1200MHz to 3000MHz (Reactive Match)	–11 –18	–5 –10	1 –2	dBm dBm

AC ELECTRICAL CHARACTERISTICS

Downmixer Applications: (Test Circuits Shown in Figures 1 and 2)
V_{CC} = 5V, EN = High, T_A = 25°C, P_{RF} = –10dBm (–10dBm/tone for two-tone IIP3 tests, ∆f = 200kHz), High-Side LO at –5dBm for 45MHz, 140MHz and 450MHz tests, Low-Side LO at –10dBm for 900MHz, 1900MHz and 2450MHz tests, unless otherwise noted. (Note 2, 3 and 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Gain	RF = 45MHz, IF = 2MHz RF = 140MHz, IF = 10MHz RF = 450MHz, IF = 70MHz RF = 900MHz, IF = 170MHz RF = 1900MHz, IF = 170MHz RF = 2450MHz, IF = 240MHz	 –1 	1 2 1.1 0 1 2		dB dB dB dB dB dB
Conversion Gain vs Temperature	T_A = –40°C to 85°C, RF = 900MHz		–0.011		dB/°C
Input 3rd Order Intercept	RF = 45MHz, IF = 2MHz RF = 140MHz, IF = 10MHz RF = 450MHz, IF = 70MHz RF = 900MHz, IF = 170MHz RF = 1900MHz, IF = 170MHz RF = 2450MHz, IF = 240MHz		20.4 20.7 21.3 21 17 13		dBm dBm dBm dBm dBm dBm
Single-Sideband Noise Figure	RF = 140MHz, IF = 10MHz RF = 450MHz, IF = 70MHz RF = 900MHz, IF = 170MHz RF = 1900MHz, IF = 170MHz RF = 2450MHz, IF = 240MHz		10.3 10.3 11 14 13.4		dB dB dB dB dB
LO to RF Leakage	f_{LO} = 250kHz to 700MHz (Figure 1) f_{LO} = 700MHz to 2500MHz (Figure 2)		≤–63 ≤–50		dBm dBm
LO to IF Leakage	f_{LO} = 250kHz to 500MHz (Figure 1) f_{LO} = 500MHz to 1250MHz (Figure 1) f_{LO} = 700MHz to 1500MHz (Figure 2) f_{LO} = 1500MHz to 1950MHz (Figure 2) f_{LO} = 1950MHz to 2500MHz (Figure 2)		≤–35 ≤–40 ≤–45 ≤–40 ≤–32		dBm dBm dBm dBm dBm
RF to LO Isolation	f_{RF} = 250kHz to 800MHz (Figure 1) f_{RF} = 700MHz to 1200MHz (Figure 2) f_{RF} = 1200MHz to 1700MHz (Figure 2) f_{RF} = 1700MHz to 2500MHz (Figure 2)		>61 >49 >46 >43		dB dB dB dB
2RF-2LO Output Spurious Product ($f_{RF} = f_{LO} + f_{IF}/2$)	900MHz: f_{RF} = 815MHz at –12dBm, f_{IF} = 170MHz 1900MHz: f_{RF} = 1815MHz at –12dBm, f_{IF} = 170MHz		–66 –59		dBc dBc
3RF-3LO Output Spurious Product ($f_{RF} = f_{LO} + f_{IF}/3$)	900MHz: f_{RF} = 786.67MHz at –12dBm, f_{IF} = 170MHz 1900MHz: f_{RF} = 1786.67MHz at –12dBm, f_{IF} = 170MHz		–83 –58		dBc dBc
Input 1dB Compression	RF = 10MHz to 500MHz (Figure 1) RF = 900MHz (Figure 2) RF = 1900MHz (Figure 2)		10.5 10.1 6.2		dBm dBm dBm

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

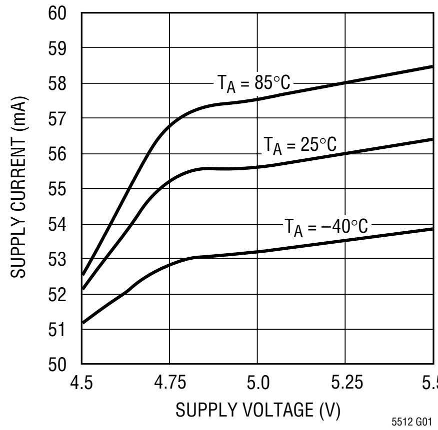
Note 2: 45MHz, 140MHz and 450MHz performance measured on the test circuit shown in Figure 1. 900MHz, 1900MHz and 2450MHz performance measured on the test circuit shown in Figure 2.

Note 3: Specifications over the –40°C to 85°C temperature range are assured by design, characterization and correlation with statistical process control.

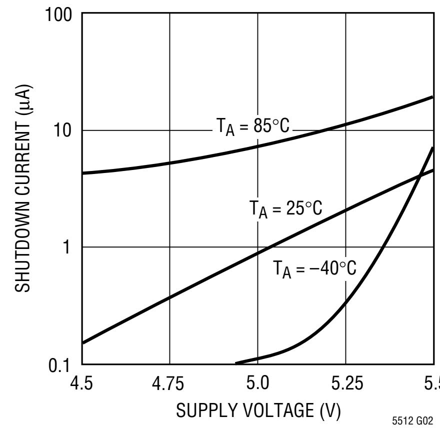
Note 4: SSB Noise Figure measurements performed with a small-signal noise source and bandpass filter on RF input and no other RF signal applied.

TYPICAL DC PERFORMANCE CHARACTERISTICS (Test Circuit Shown Figure 2)

Supply Current vs Supply Voltage



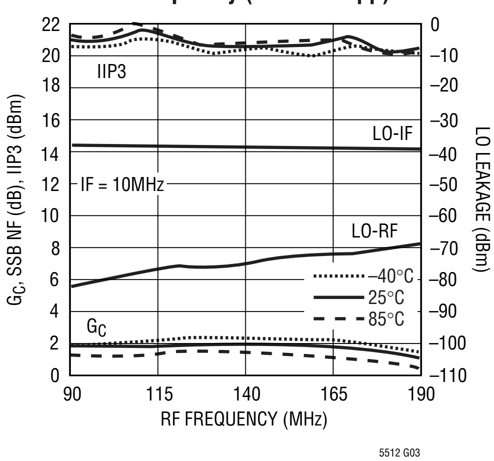
Shutdown Current vs Supply Voltage



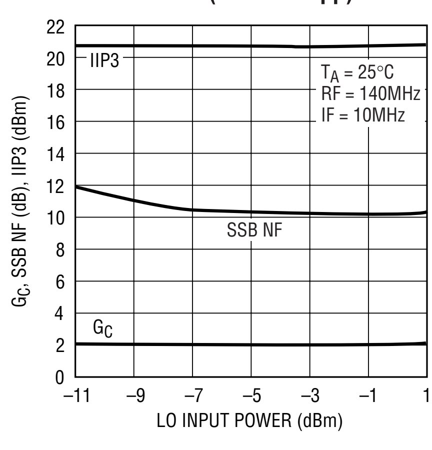
TYPICAL AC PERFORMANCE CHARACTERISTICS HF/VHF/UHF Downmixer Application

V_{CC} = 5V, EN = High, P_{RF} = –10dBm (–10dBm/tone for 2-tone IIP3 tests, Δf = 200kHz), High-Side LO, P_{LO} = –5dBm, unless otherwise noted. Test Circuit Shown in Figure 1.

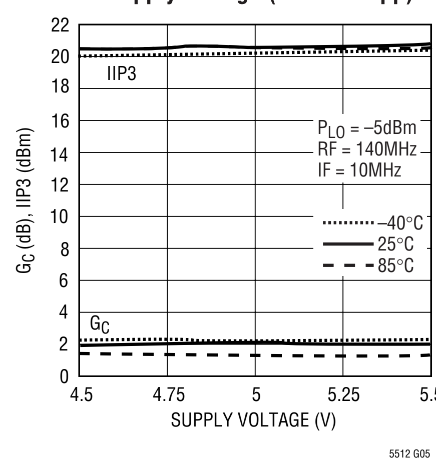
Conv Gain, IIP3 and LO Leakage vs RF Frequency (140MHz App)



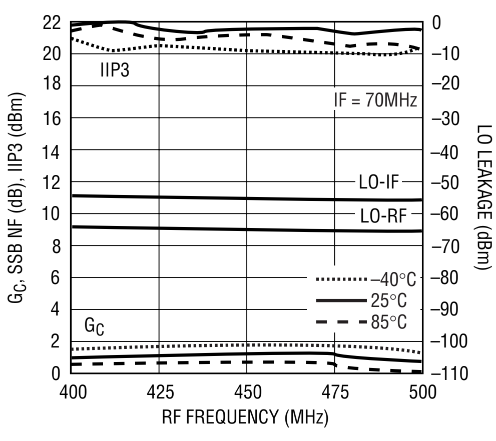
Conv Gain, IIP3 and NF vs LO Power (140MHz App)



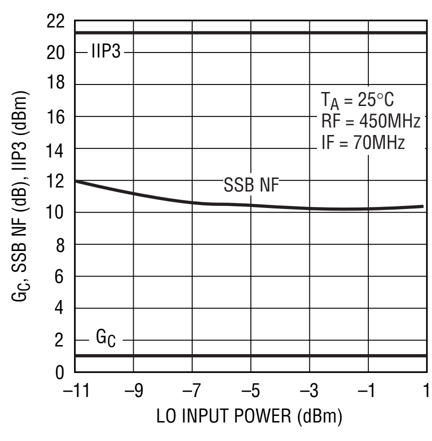
Conv Gain and IIP3 vs Supply Voltage (140MHz App)



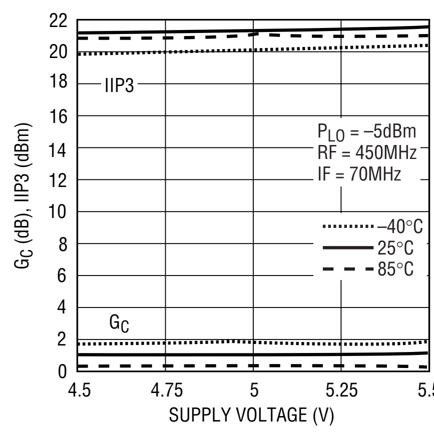
Conv Gain, IIP3 and LO Leakage vs RF Frequency (450MHz App)



Conv Gain, IIP3 and NF vs LO Power (450MHz App)



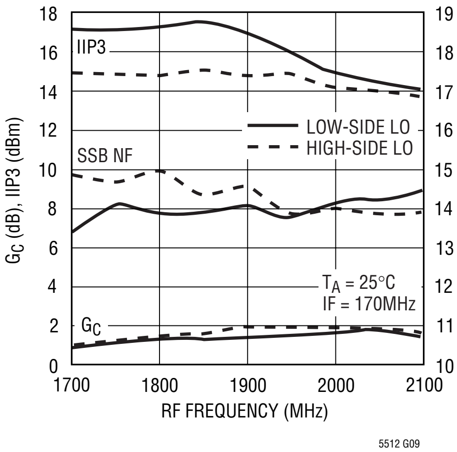
Conv Gain and IIP3 vs Supply Voltage (450MHz App)



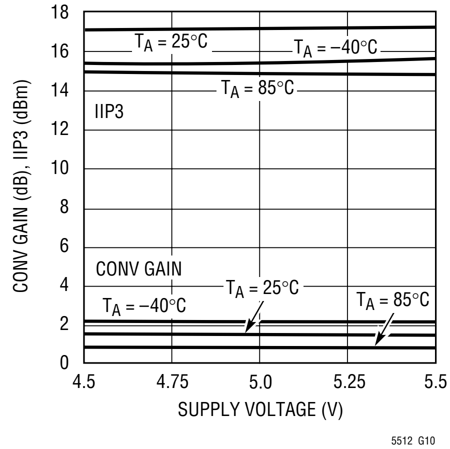
TYPICAL PERFORMANCE CHARACTERISTICS (1900MHz Downmixer Application)

V_{CC} = 5V, EN = High, T_A = 25°C, 1900MHz RF input matching, P_{RF} = –10dBm (–10dBm/tone for 2-tone IIP3 tests, ∆f = 200kHz), Low-Side LO, P_{LO} = –10dBm, IF output measured at 170MHz, unless otherwise noted. Test circuit shown in Figure 2.

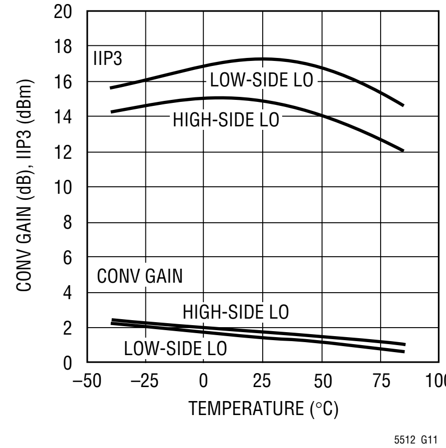
Conv Gain, IIP3 and NF vs RF Frequency



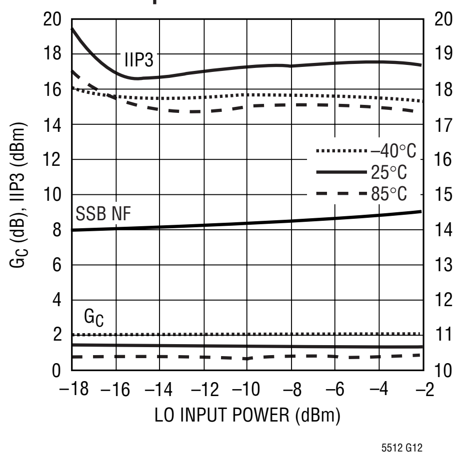
Conv Gain and IIP3 vs Supply Voltage



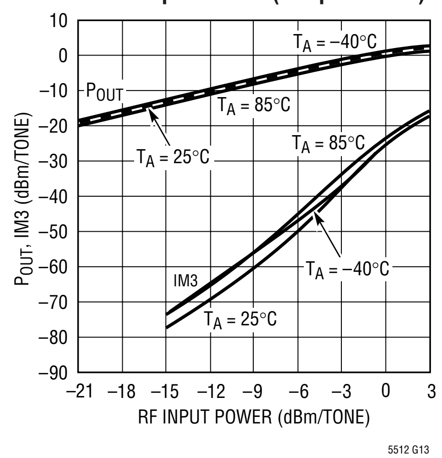
Conv Gain and IIP3 vs Temperature RF = 1900MHz, IF = 170MHz



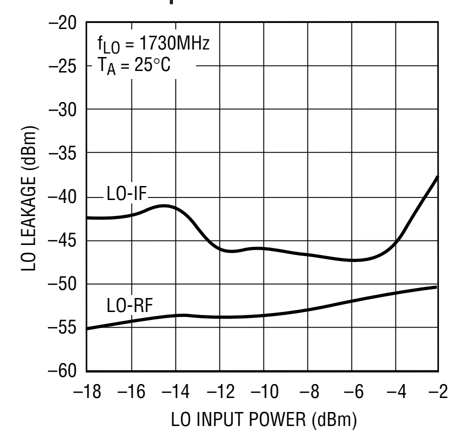
Conv Gain, IIP3 and NF vs LO Input Power



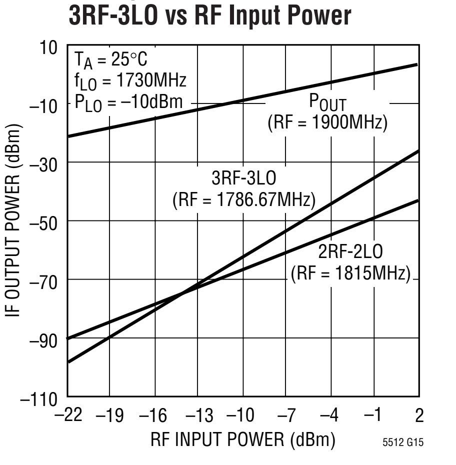
Output IF Power and Output IM3 vs RF Input Power (2 Input Tones)



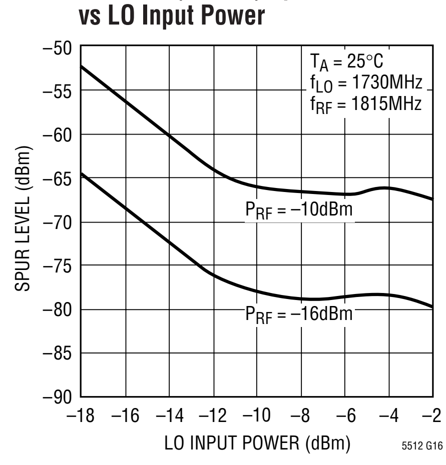
LO-IF and LO-RF Leakage vs LO Input Power



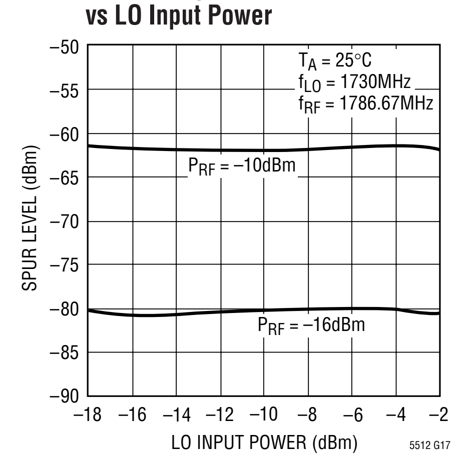
IF Output Power, 2RF-2LO and 3RF-3LO vs RF Input Power



2RF-2LO (Half-IF) Spur Level vs LO Input Power



3RF-3LO Spur Level vs LO Input Power



PIN FUNCTIONS

NC (Pins 1, 4, 8, 13, 16): Not connected internally. These pins should be grounded on the circuit board for improved LO to RF and LO to IF isolation.

RF+, RF– (Pins 2, 3): Differential Inputs for the RF Signal. These pins must be driven with a differential signal. Each pin must be connected to a DC ground capable of sinking 15mA (30mA total). This DC bias return can be accomplished through the center-tap of a balun, or with shunt inductors. An impedance transformation is required to match the RF input to 50Ω (or 75Ω).

EN (Pin 5): Enable Pin. When the input voltage is higher than 3V, the mixer circuits supplied through Pins 6, 7, 10, and 11 are enabled. When the input voltage is less than 0.3V, all circuits are disabled. Typical enable pin input current is 50μA for EN = 5V and 0μA when EN = 0V.

V_{CC1} (Pin 6): Power Supply Pin for the LO Buffer Circuits. Typical current consumption is 22mA. This pin should be externally connected to the other V_{CC} pins, and decoupled with 0.01μF and 1μF capacitors.

V_{CC2} (Pin 7): Power Supply Pin for the Bias Circuits. Typical current consumption is 4mA. This pin should be externally connected to the other V_{CC} pins, and decoupled with 0.01μF and 1μF capacitors.

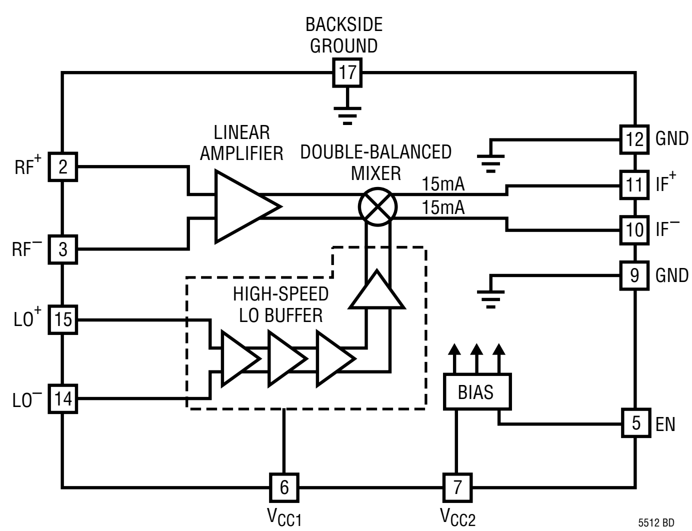
GND (Pins 9 and 12): Ground. These pins are internally connected to the backside ground for better isolation. They should be connected to RF ground on the circuit board, although they are not intended to replace the primary grounding through the backside contact of the package.

IF–, IF+ (Pins 10, 11): Differential Outputs for the IF Signal. An impedance transformation may be required to match the outputs. These pins must be connected to V_{CC} through impedance matching inductors, RF chokes or a transformer center-tap.

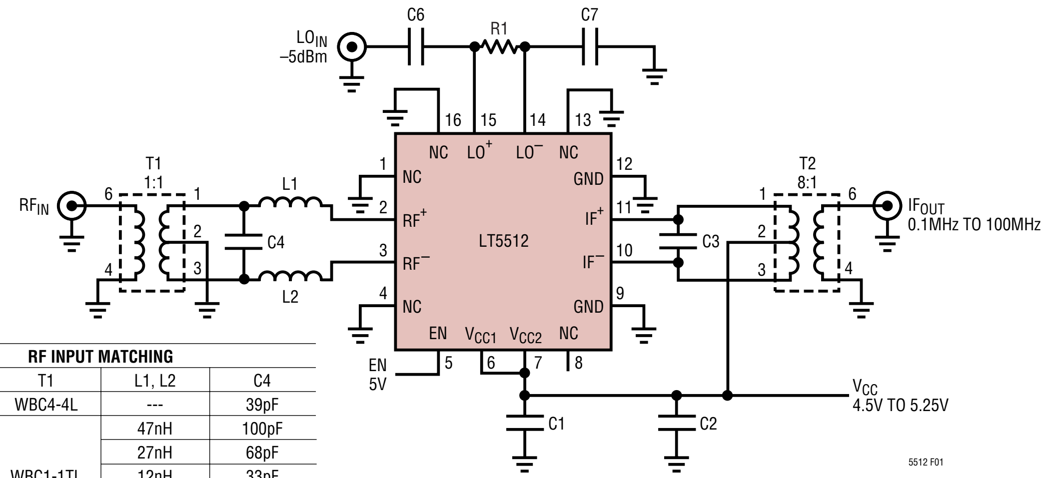
LO–, LO+ (Pins 14, 15): Differential Inputs for the Local Oscillator Signal. They can also be driven single-ended by connecting one to an RF ground through a DC blocking capacitor. These pins are internally biased to 2V; thus, DC blocking capacitors are required. An impedance transformation or matching resistor is required to match the LO input to 50Ω (or 75Ω).

GROUND (Pin 17): (Backside Contact): Circuit Ground Return for the Entire IC. This must be soldered to the printed circuit board ground plane.

BLOCK DIAGRAM



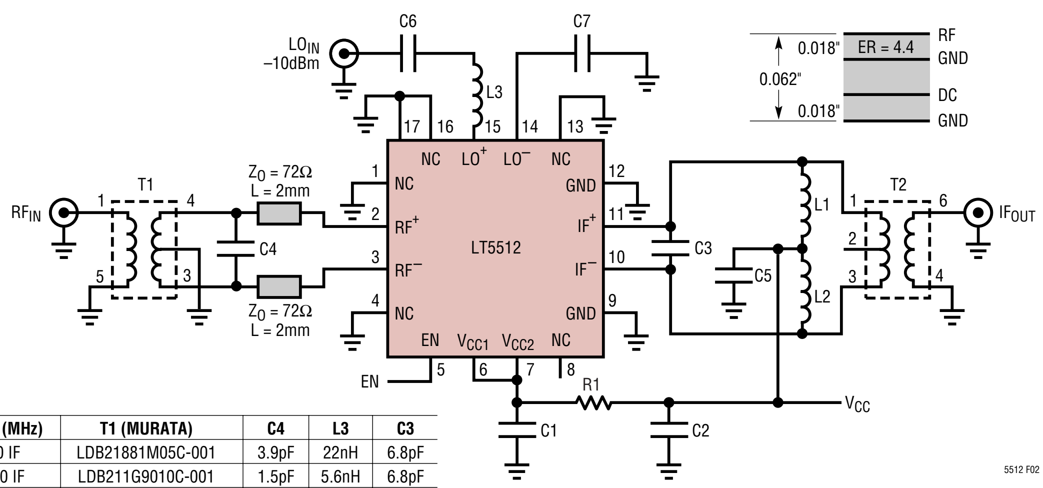
TEST CIRCUITS



RF INPUT MATCHING			
RF(MHz)	T1	L1, L2	C4
0.25 - 250	WBC4-4L	---	39pF
45	WBC1-1TL	47nH	100pF
70		27nH	68pF
140		12nH	33pF
240		6.8nH	18pF
380		5.6nH	12pF
450		4.7nH	10pF

REF DES	VALUE	SIZE	PART NUMBER	REF DES	VALUE	SIZE	PART NUMBER
R1	100Ω	0402	AAC CR05-101J	C4	See Table	0402	AVX 0402
C1, C6, C7	0.01µF	0402	AVX 04023C103JAT	L1, L2	See Table	0402	Toko LL1005-FH
C2	1µF	0603	AVX 0603ZD105KAT	T1	1:1		Coilcraft WBC1-1TL
C3	1.8pF	0402	AVX 04025A1R8BAT	T2	8:1		Mini-Circuits TC8-1

Figure 1. Test Schematic for HF/VHF/UHF Downmixer Applications



APPLICATION (MHz)	T1 (MURATA)	C4	L3	C3
900 RF/170 IF	LDB21881M05C-001	3.9pF	22nH	6.8pF
1900 RF/170 IF	LDB211G9010C-001	1.5pF	5.6nH	6.8pF
2450 RF/240 IF	LDB212G4020C-001	1.2pF	4.7nH	3.3pF

REF DES	VALUE	SIZE	PART NUMBER	REF DES	VALUE	SIZE	PART NUMBER
C5, C6, C7	100pF	0402	Murata GRP1555C1H101J	L1, L2	47nH	0402	Coilcraft 0402CS-47NX
C1	0.01µF	0402	Murata GRP155R71C103K	L3	See Table	0402	Toko LL1005-FH
C2	1.0µF	0603	Taiyo Yuden LMK107F105ZA	R1	10	0402	
C4	See Table	0402	Murata GRP1555C	T1	See Table		Murata LDB21 Series
C3	See Table	0402	Murata GRP1555C	T2	8:1		Mini-Circuits TC8-1

Figure 2. Test Schematic for 900MHz to 2.5GHz Downmixer Applications

APPLICATIONS INFORMATION

The LT5512 consists of a double-balanced mixer, RF buffer amplifier, high-speed limiting LO buffer and bias/enable circuits. The differential RF, LO and IF ports require simple external matching which allows the mixer to be used at very low frequencies, below 1MHz, or up to 3GHz. Low side or high side LO injection can be used.

Two evaluation circuits are available. The HF/VHF/UHF evaluation circuit is shown in Figure 1 and the 900MHz to 2.5GHz evaluation circuit is shown in Figure 2. The corresponding demo board layouts are shown in Figures 10 and 11, respectively.

RF Input Port

A simplified schematic of the differential RF input is shown in Figure 3, with the associated external impedance matching elements for a 450MHz application. Each RF input requires a low resistance DC return to ground capable of sinking 15mA. This can be accomplished with the center-tap of a balun as shown in Figure 3, or with bias chokes connected from Pins 2 and 3 to ground, if a differential RF input signal is available. The value of the bias chokes should be high enough to avoid reducing the input impedance at the frequency of interest.

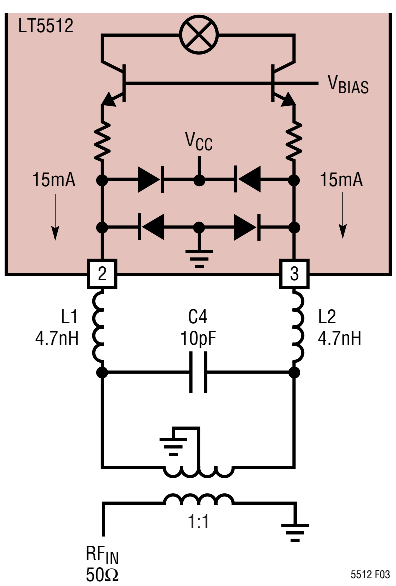


Figure 3. RF Input with External Matching for a 450MHz Application

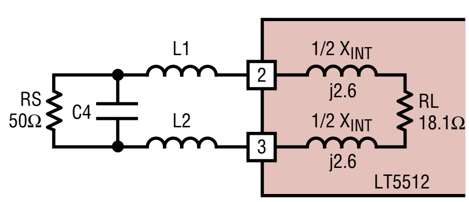


Figure 4. 450MHz RF Input Matching

Table 1 lists the differential input impedance and differential reflection coefficient between Pins 2 and 3 for several common RF frequencies. As shown in Figures 3 and 4, low-pass impedance matching is used to transform the differential input impedance up to the desired value for the balun input. The following example shows how to design the low-pass impedance transformation network for the RF input.

From Table 1, the differential input impedance at 450MHz is 18.1 + j5.2. As shown in Figure 4, the 5.2Ω reactance is split, with one half on each side of the 18.1Ω load resistor. The matching network will consist of additional inductance in series with the internal inductance and a capacitor in parallel with the desired 50Ω source impedance. The capacitance (C4) and inductance are calculated as follows.

$$Q = \sqrt{(R_S / R_L) - 1} = \sqrt{(50/18.1) - 1} = 1.328$$

$$C4 = \frac{Q}{\omega R_S} = \frac{1.328}{2\pi \cdot 450\text{MHz} \cdot 50} = 9.4\text{pF (use 10pF)}$$

$$L1, L2 = \frac{R_L \cdot Q}{2\omega} = \frac{18.1 \cdot 1.328}{2 \cdot 2\pi \cdot 450\text{MHz}}$$

$$= 4.2\text{nH (use 4.7nH)}$$

Table 1. RF Input Differential Impedance

Frequency (MHz)	Differential Input Impedance	Differential S11	
		Mag	Angle
10	18.2 + j0.14	0.467	179.6
44	18 + j0.26	0.470	178.6
240	18.1 + j2.8	0.471	172.6
450	18.1 + j5.2	0.473	166.3
950	18.7 + j11.3	0.479	150.8
1900	20.6 + j22.8	0.503	124.3
2150	21.4 + j26.5	0.512	116.9
2450	22.5 + j30.5	0.522	109.2
2700	24.1 + j34.7	0.530	101.7

APPLICATIONS INFORMATION

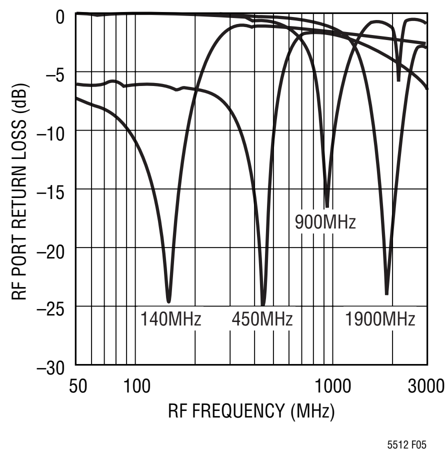


Figure 5. RF Input Return Loss (140MHz, 450MHz, 900MHz and 1900MHz Matching)

At high frequencies (greater than 900MHz), this same matching technique is used, but it is important to consider the IC's input reactance when calculating the external inductance. As shown in Figure 2, the high-frequency evaluation board uses short (2mm) 72Ω microstrip lines to realize the required inductance, instead of chip inductors.

External matching values for several frequencies, ranging from 45MHz to 2.45GHz are shown in Figures 1 and 2. Measured RF input return losses are plotted in Figure 5.

LO Input Port

The LO buffer amplifier consists of high-speed limiting differential amplifiers, designed to drive the mixer quad for high linearity. The LO^+ and LO^- pins are designed for differential or single-ended drive. Both LO pins are internally biased to $2V_{DC}$.

Table 2. LO Input Differential Impedance

Frequency (MHz)	Differential Input Impedance	Differential S11	
		Mag	Angle
750	263 + j172	0.766	–10.2
1000	213 + j178	0.760	–13.4
1250	175 + j173	0.752	–16.6
1500	146 + j164	0.743	–19.8
1750	125 + j153	0.733	–22.8
2000	108 + j142	0.722	–25.8
2250	95 + j131	0.709	–28.9
2500	86 + j122	0.695	–31.8
2750	78 + j133	0.68	–34.6

A simplified schematic of the LO input is shown in Figure 6 with simple resistive matching and DC blocking capacitors. This is the preferred matching for LO frequencies below 1.5GHz. The internal (DC) resistance is 400Ω. The required LO drive at the IC is $150mV_{RMS}$ (typical) which can come from a 50Ω source, or a higher impedance source such as PECL. The external matching resistor is required only to reduce the amplitude of the LO signal at the IC, although the input stage will tolerate 10dB of overdrive without significant performance degradation. Resistive LO port matching is used on the low-frequency evaluation board (see Figure 1).

Above 1.5GHz, the internal capacitance becomes significant and reactive matching to 50Ω with a single series inductor and DC blocking capacitors is preferred. A schematic is shown in Figure 7. Table 2 lists the differential input

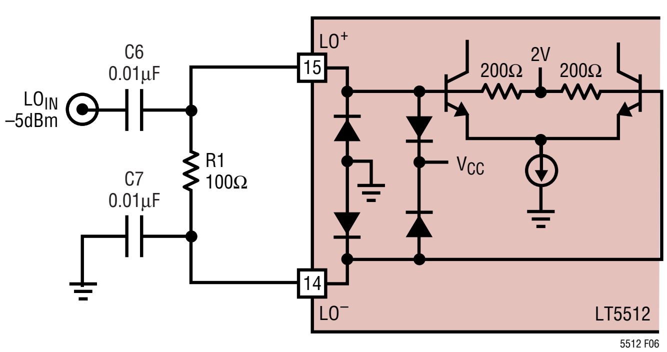


Figure 6. LO Input with Resistive Matching

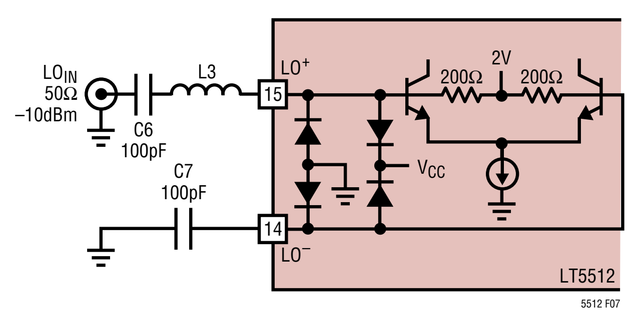


Figure 7. LO Input with Reactive Matching

APPLICATIONS INFORMATION

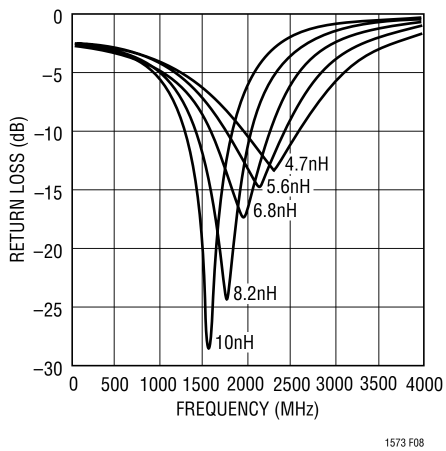


Figure 8. Single-Ended LO Port Return Loss vs Frequency for Various Values of L3

impedance and differential reflection coefficient between the LO+ and LO– pins. This information can be used to compute the value of the series matching inductor, L3. Alternatively, Figure 8 shows measured LO input return loss versus frequency for various values of L3. Reactive LO port matching is used on the high-frequency evaluation board (see Figure 2).

IF Output Port

The differential IF outputs, IF+ and IF–, are internally connected to the collectors of the mixer switching transistors as shown in Figure 9. These outputs should be combined externally through an RF balun or 180° hybrid to achieve optimum performance. Both pins must be biased at the supply voltage, which can be applied through matching inductors (see Figure 2), or through the center-tap of an output transformer (see Figure 1). These pins are protected with ESD diodes; the diodes allow peak AC signal swing up to 1.3V above V_{CC}.

As shown in Table 3, the IF output differential impedance is approximately 390Ω in parallel with 0.44pF. A simple band-pass IF matching network suitable for wireless applications is shown in Figure 9. Here, L1, L2 and C3 set the desired IF output frequency. The 390Ω differential output can then be applied directly to a differential filter, or an 8:1 balun for impedance transformation down to 50Ω. To achieve maximum linearity, C3 should be located as close as possible to the IF+/IF– pins. Even small amounts of inductance in series with C3 (such as through a via) can significantly degrade IIP3. The value of C3 should be reduced by the value of internal capacitance (see Table 3). This matching network is simple and offers good selectivity for narrow band IF applications.

For IF frequencies below 100MHz, the simplest IF matching technique is an 8:1 transformer connected across the IF pins as shown in Figure 1. DC bias to the IF+ and IF– pins is provided through the transformer's center-tap. A small value IF capacitor (C3) improves the LO-IF leakage and attenuates the undesired image frequency. No inductors are required.

Table 3. IF Output Differential Impedance (Parallel Equivalent)

Frequency (MHz)	Differential Output Impedance	Differential S11	
		Mag	Angle
10	396 II - j10k	0.766	0
70	394 II - j5445	0.775	–1.1
170	393 II - j2112	0.774	–2.8
240	392 II - j1507	0.773	–3.9
450	387 II - j798	0.772	–7.3
750	377 II - j478	0.768	–12.2
860	371 II - j416	0.766	–14.0
1000	363 II - j359	0.762	–16.2
1250	363 II - j295	0.764	–19.6
1500	346 II -j244	0.756	–23.6
1900	317 II - j192	0.743	–29.9

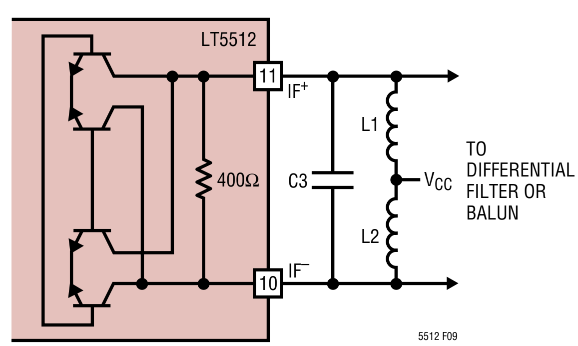
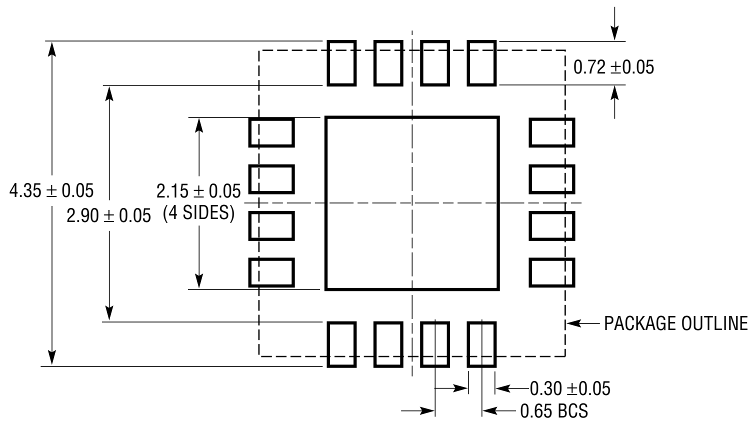


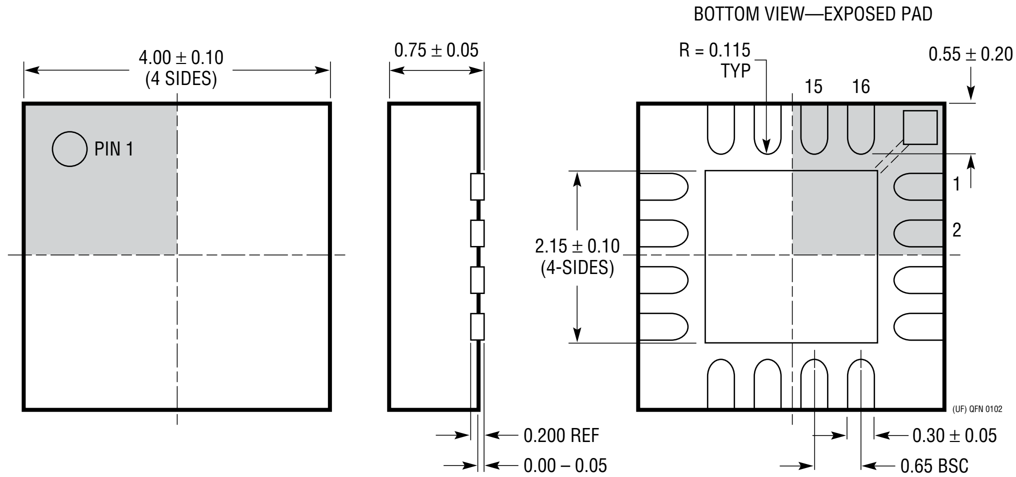
Figure 9. IF Output Equivalent Circuit with Band-Pass Matching Elements

PACKAGE DESCRIPTION

UF Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. EXPOSED PAD SHALL BE SOLDER PLATED

APPLICATIONS INFORMATION

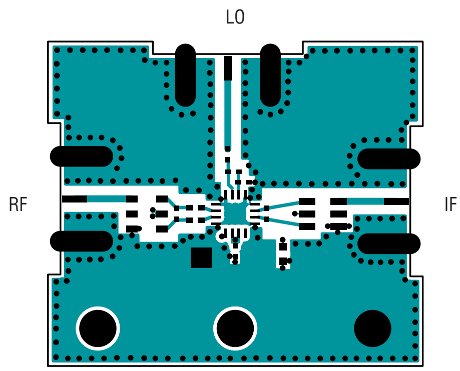


Figure 10. HF/VHF/UHF Evaluation Board Layout (DC933A)

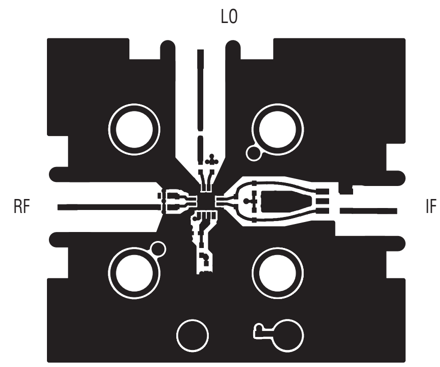


Figure 11. High-Frequency Evaluation Board Layout (DC478B)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Infrastructure		
LT5511	High Linearity Upconverting Mixer	RF Output to 3GHz, 17dBm IIP3, Integrated LO Buffer
LT5514	Ultralow Distortion, IF Amplifier/ADC Driver with Digitally Controlled Gain	850MHz Bandwidth, 47dBm OIP3 at 100MHz, 10.5dB to 33dB Gain Control Range
LT5515	1.5GHz to 2.5GHz Direct Conversion Quadrature Demodulator	20dBm IIP3, Integrated LO Quadrature Generator
LT5516	0.8GHz to 1.5GHz Direct Conversion Quadrature Demodulator	21.5dBm IIP3, Integrated LO Quadrature Generator
LT5517	40MHz to 900MHz Quadrature Demodulator	21dBm IIP3, Integrated LO Quadrature Generator
LT5519	0.7GHz to 1.4GHz High Linearity Upconverting Mixer	17.1dBm IIP3 at 1GHz, Integrated RF Output Transformer with 50Ω Matching, Single-Ended LO and RF Ports Operation
LT5520	1.3GHz to 2.3GHz High Linearity Upconverting Mixer	15.9dBm IIP3 at 1.9GHz, Integrated RF Output Transformer with 50Ω Matching, Single-Ended LO and RF Ports Operation
LT5521	10MHz to 3700MHz High Linearity Upconverting Mixer	24.2dBm IIP3 at 1.95GHz, NF = 12.5dB, 3.15V to 5.25V Supply, Single-Ended LO Port Operation
LT5522	400MHz to 2.7GHz High Signal Level Downconverting Mixer	4.5V to 5.25V Supply, 25dBm IIP3 at 900MHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports
LT5524	Low Power, Low Distortion ADC Driver with Digitally Programmable Gain	450MHz Bandwidth, 40dBm OIP3, 4.5dB to 27dB Gain Control
LT5525	High Linearity, Low Power Downconverting Mixer	Single-Ended 50Ω RF and LO Ports, 17.6dBm IIP3 at 1900MHz, I_{CC} = 28mA
LT5526	High Linearity, Low Power Downconverting Mixer	3V to 5.3V Supply, 16.5dBm IIP3, 100kHz to 2GHz RF, NF = 11dB, I_{CC} = 28mA, –65dBm LO-RF Leakage
LT5527	400MHz to 3.7GHz High Signal Level Downconverting Mixer	Single-Ended 50Ω RF and LO Ports, 23.5dBm IIP3 at 1.9GHz
LT5528	1.5GHz to 2.4GHz High Linearity Direct I/Q Modulator	21.8dBm OIP3 at 2GHz, –159dBm/Hz Noise Floor, 50Ω Interface at all Ports

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